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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,607	10/13/2003	Herbert L. Ho	FIS920030214US1	2606

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EXAMINER
CHEN, ERIC BRICE

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,607	HO ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/13/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kleinhenz (U.S. Patent No. 5,770,484).

4. As to claim 1, Kleinhenz discloses a method for etching a silicon on insulator (SOI) substrate, the method comprising: opening (column 4, lines 12-15) a hardmask layer (130/140/150) (column 3, lines 66-67; column 4, lines 1-9) formed on an SOI layer (120) of the SOI substrate (100/110) (column 3, lines 40-

42); etching through said SOI layer (120), a buried insulator layer (110) underneath said SOI layer, and a bulk silicon layer (100) beneath said insulator layer a single etch step (column 4, lines 12-22; Figure 4).

5. As to claim 10, Kleinhenz discloses a method for forming a deep trench within a silicon on insulator (SOI) substrate, the method comprising: forming a hardmask layer (130/140/150) (column 3, lines 66-67; column 4, lines 1-9) on an SOI layer (120) of the SOI substrate (100/110) (column 3, lines 40-42); patterning a desired deep trench pattern in said maskmask layer (column 4, lines 12-15; Figure 4); and etching through said SOI layer (120), a buried oxide (BOX) layer (110) underneath said SOI layer, and a bulk silicon layer (100) beneath said BOX layer using a single etch step (column 4, lines 12-22; Figure 4).

6. Claims 1-2 and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Sell et al. (U.S. Patent Appl. No. 2004/0147074).

7. As to claim 1, Sell discloses a method for etching a silicon on insulator (SOI) substrate, the method comprising: opening a hardmask layer formed on an SOI layer (47) of the SOI substrate (41) (paragraph 0076; Figure 8); etching through said SOI layer (47), a buried insulator layer (46) underneath said SOI layer, and a bulk silicon layer (41) beneath said insulator layer a single etch step (paragraph 0076; Figure 9).

8. As to claim 2, Sell discloses that etching is implemented with an HBr, NF_3 and O_2 etch chemistry (paragraph 0076).

9. As to claim 10, Sell discloses a method for forming a deep trench within a silicon on insulator (SOI) substrate, the method comprising: forming a hardmask

layer on an SOI layer (47) of the SOI substrate (41) (paragraph 0076; Figure 8); patterning a desired deep trench pattern in said maskmask layer (paragraph 0076; Figure 8); and etching through said SOI layer (47), a buried oxide (BOX) layer (46) underneath said SOI layer, and a bulk silicon layer (41) beneath said BOX layer using a single etch step (paragraph 0076; Figure 9).

10. As to claim 11, Sell discloses that etching is implemented with an HBr, NF_3 and O_2 etch chemistry (paragraph 0076).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3-4 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sell, in view of Rossnagel et al., Handbook of Plasma Processing, Noyes Publications (1990).

13. As to claims 3 and 11, Sell does not expressly disclose that the etch chemistry is applied at a power of about 500 to about 1,000 Watts. However, Rossnegal summarizes the typical characteristics for plasma etching (Table 1, page 198), including a power density of 0.05-1.0 W/cm^2 (or a power range of about 35-700 W for a 300 mm wafer). It should be noted that applicants' claimed power range falls within the conventional range taught by Rossnegal. Therefore,

it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a power range of about 500 to about 1,000 Watts. One of ordinary skill in the art would have been motivated to select this range, because it is known to successfully accomplish plasma etching.

14. As to claim 4 and 12, Sell does not expressly disclose that the etching is implemented at a pressure of about 10 to about 150 mTorr. However, Rossnegal summarizes the typical characteristics for plasma etching (Table 1, page 198), including a gas pressure of 10-200 mTorr. It should be noted that applicants' claimed gas pressure falls within the conventional ranges taught by Rossnegal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a gas pressure range of about 10 to about 150 mTorr. One of ordinary skill in the art would have been motivated to select this range, because it is known to successfully accomplish plasma etching.

15. Claims 5-9 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sell, in view of Wolf, Silicon Processing for the VLSI Era, Vols. 1 and 4; Lattice Press (1986, 2002).

16. As to claims 5, Sell does not expressly disclose that the hardmask layer is formed at a thickness so as to accommodate a 1:1 etch selectivity with respect to said buried insulator layer and selectivity with respect about a 5:1 to about a 35:1 etch to said SOI layer and said bulk silicon layer. Wolf teaches that both the mask material and underlying layer materials are generally etchable and that selectivity is the ratio of the of etch rates of different materials. Etch selectivity with respect to the mask material plays a role in the etched size features. Wolf

also teaches that overall film thickness (or depth of an etched feature) influences etch selectivity (vol. 1, page 523), such that etching a thicker film (or deeper feature) requires a thicker etch mask (vol. 1, page 524, Figure 7). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of forming the hardmask layer at a thickness so as to accommodate a 1:1 etch selectivity with respect to said buried insulator layer and selectivity with respect about a 5:1 to about a 35:1 etch to said SOI layer and said bulk silicon layer. One who is skilled in the art would be motivated to form a hardmask layer of appropriate thickness, such that the hardmask layer is not completely removed by etching, prior to etching a feature to its desired depth.

17. As to claim 6, Sell discloses that the hardmask layer further comprises: a pad nitride layer (44) formed on said SOI layer (47); and a borosilicate glass (BSG) oxide layer formed on said pad nitride layer (paragraph 0076; Figure 8).

18. As to claim 7, Sell discloses that the hardmask layer is formed at a thickness of about 6,000 Å to about 20,000 Å (paragraph 0076). The total thickness of the hardmask layer is the total thickness of layers (44) and BSG layer. Layer (44) is 200 nm thick; BSG layer is 1,000 nm thick. The total thickness of the hardmask is 1,200 nm (12,000 Å).

19. As to claim 8, Sell discloses that the hardmask layer is formed at a thickness of about 10,000 Å to about 18,000 Å (paragraph 0076).

20. As to claim 9, Sell discloses that the buried insulator layer (46) comprises a buried oxide (BOX) layer (paragraph 0076), but does not expressly disclose

that the BOX layer is formed at a thickness of about 120 to about 140 nanometers. However, Wolf teaches that for silicon-on-insulator technology, a typical range for the thickness of the BOX layer is 90-150 nm (vol. 4, pages 535-36). It should be noted that applicants' claimed BOX thickness falls within the conventional thickness range taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a BOX thickness of about 120 to about 140 nanometers. One of ordinary skill in the art would have been motivated to select this conventional thickness range, because it is known to successfully produce a silicon-on-insulator device.

21. As to claims 14, Sell does not expressly disclose that the hardmask layer is formed at a thickness so as to accommodate a 1:1 etch selectivity with respect to said BOX layer and selectivity with respect about a 5:1 to about a 35:1 etch to said SOI layer and said bulk silicon layer. Wolf teaches that both the mask material and underlying layer materials are generally etchable and that selectivity is the is the ratio of the of etch rates of different materials. Etch selectivity with respect to the mask material plays a role in the etched size features. Wolf also teaches that overall film thickness (or depth of an etched feature) influences etch selectivity (vol. 1, page 523), such that etching a thicker film (or deeper feature) requires a thicker etch mask (vol. 1, page 524, Figure 7). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of forming the hardmask layer at a thickness so as to accommodate a 1:1 etch selectivity with respect to said BOX layer and selectivity with respect about a 5:1 to about a 35:1 etch to said SOI layer and said bulk

silicon layer. One who is skilled in the art would be motivated to form a hardmask layer of appropriate thickness, such that the hardmask layer is not completely removed by etching, prior to etching a feature to its desired depth.

22. As to claim 15, Sell discloses that the hardmask layer further comprises: a pad nitride layer (44) formed on said SOI layer (47); and a borosilicate glass (BSG) oxide layer formed on said pad nitride layer (paragraph 0076; Figure 8).

23. As to claim 16, Sell discloses that the hardmask layer is formed at a thickness of about 6,000 Å to about 20,000 Å (paragraph 0076).

24. As to claim 17, Sell discloses that the hardmask layer is formed at a thickness of about 10,000 Å to about 18,000 Å (paragraph 0076).

25. As to claim 18, Sell discloses that the buried insulator layer (46) comprises a buried oxide (BOX) layer (paragraph 0076), but does not expressly disclose that the BOX layer is formed at a thickness of about 120 to about 140 nanometers. However, Wolf teaches that for silicon-on-insulator technology, a typical range for the thickness of the BOX layer is 90-150 nm (vol. 4, pages 535-36). It should be noted that applicants' claimed BOX thickness falls within the conventional thickness range taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a BOX thickness of about 120 to about 140 nanometers. One of ordinary skill in the art would have been motivated to select this conventional thickness range, because it is known to successfully produce a silicon-on-insulator device.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shen (U.S. Patent No. 6,472,702) discloses a method of etching a SOI substrate with HBr, NF_3 and O_2 etching gases.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC
Jan. 27, 2005

EBC

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER